SESSION 17 – TAPA I
Serial Link Components

Friday, June 18, 3:25 p.m.
Chairpersons: W. Lee, Texas Instruments
M. Mizuno, NEC

17.1 — 3:25 p.m.
A Six Phases LC Based Ring Oscillator for 1.5-3GBit/s SATA Interface, R. Tonietto, I. Bietti*, B. Mercier**, R. Marbot**, and R. Castello, Università di Pavia, Pavia, Italy, *STMicroelectronics, Pavia, Italy, **STMicroelectronics, Grenoble, France

A 3GHz six phases PLL clock synthesizer embedded in a complete Serial Advanced Technology Attachment standard compliant oversampling PHY is presented. Multiphase frequency synthesis has been realized using an LC ring structure VCO, featuring improved phase noise and phase accuracy. Integrated in a standard 0.13um CMOS process the synthesizer has an area of 0.8 square mm and burns 35mW while achieving a phase noise of -120dBc/Hz@1MHz and a maximum measured phase error of 0.3 degree.

17.2 — 3:50 p.m.
Burst Mode Packet Receiver using a Second Order DLL, H. Lee, C.H. Yue, S. Palermo, K.W. Mai and M. Horowitz, Stanford University, Stanford, CA

This paper describes a CDR that can be used to receive optically switched packets. Rather than using fast phase acquisition to lock onto each packet, it uses a second order delay locked loop to acquire both the frequency and phase of each source to predict future bit transitions. A 0.25μm CMOS prototype can track frequency offsets of 100ppm to better than 0.1ppm and can retain lockon 10Kbit 3.125Gbps packets that occur once every 2.4Mbits.

17.3 — 4:15 p.m.
A 12.5Gbps Half-Rate CMOS CDR Circuit for 10Gbps Network Applications, J. Takasoh, T. Yoshimura, H. Kondoh and N. Higashisaka, Mitsubishi Electric Corporation, Hyogo, Japan

This paper describes a true half-rate CMOS CDR circuit suitable for 10Gbps network applications. The CDR adopts a phase detector and a current mode EXOR charge pump with alleviated switching speeds to obtain higher speed margins. A 10.3Gbps CDR for 10Gbps Ethernet has been fabricated using a 0.10μm SOI-CMOS process technology. With proposed circuit configuration, the CDR can operate over 12Gbps without error. The jitter tolerance at 10.7Gbps is more than 0.39UI with 4M-80MHz jitter frequency range.

17.4 — 4:40 p.m.
A 20Gb/s 0.13μm CMOS Serial Link Transmitter Using an LC-PLL to Directly Drive the Output Multiplexer, P. Chiang, W.J. Dally, M.-J.E. Lee*, R. Senthinathan*, Y. Oh and M. Horowitz, Stanford University, Stanford, CA, *ATI Technologies, Inc., Santa Clara, CA

A 20Gb/s transmitter is implemented in 0.13um CMOS technology. Eight 2.5Gb/s data streams are 4:1 multiplexed, sampled, and retimed into two 10Gb/s data streams. A final 20Gb/s 2:1 output multiplexer, clocked by complementary phases of an LC-VCO in a phase-locked loop, creates 20Gb/s data. The VCO is integrated with the output multiplexer, resonating the load and eliminating the need for clock buffers. Power, die area, and jitter are 165mW, 650um x 350um, and 2.37ps(RMS)/15ps(pk-pk), respectively.

17.5 — 5:05 p.m.
A 600MS/s, 5-bit Pipelined Analog-to-Digital Converter for Serial-Link Applications, A. Varzaghani and C.-K.K. Yang, University of California, Los Angeles, CA

Design of a high-speed low-to-medium resolution analog-to-digital converter with closed-loop pipeline structure has been investigated. We demonstrate a single-path 600MS/s, 5-bit ADC. It is optimally designed to meet the requirements of a serial-link receiver. For high input-bandwidth, total input-capacitance is only 170fF. At high frequencies, to improve resolution beyond the amplifier-settling limit, the reference voltage of each pipeline-stage is digitally tuned. The chip is fabricated in 0.18μm CMOS technology and consumes 70mW at 1.8V power-supply.